Nanowire-based active matrix backplanes for the control of large area X-ray imagers

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Nanowire-based active matrix backplanes for the control of large area X-ray imagers

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ABSTRACT: In digital X-ray sensors, pixel complexity is limited by the instabilities of amorphous silicon transistors or by the lack of homogeneity of their polycrystalline silicon counterparts. Here, we present a novel approach to the fabrication of thin-film transistors, based on the use of silicon nanowires grown in porous alumina templates. Transistors made from silicon nanowires are essentially studied for the post- MOS era and they exhibit excellent transport characteristics. The technology we propose is simple, as it only employs chemical vapour deposition processes for transistor fabrication. Also, as far as active matrix fabrication is concerned, a small number of masks is needed and we present a 5 mask process for the fabrication of an X-ray panel with pixel amplification.

KEYWORDS: X-ray imagers; Nanowires; Porous anodic alumina

1. Introduction

Digital X-ray sensors are increasingly being used for medical imaging applications, including radiography, mammography and fluoroscopy. Amorphous silicon technology, derived from the liquid crystal display industry, is presently used for the fabrication of the active matrix transistors that control large-area X-ray sensors. One transistor per pixel is typically needed. However, because the requirements for radiography and fluoroscopy are drastically different, more complex pixel designs would be necessary in the future, in particular for the purpose of signal amplification at pixel level [1,2]. Thin-film transistors (TFTs) based on amorphous silicon are known to exhibit severe gate voltage instabilities, particularly when their duty cycle is high [3], making them difficult to use for any other electronic function than switching.

Polycrystalline silicon technology also suffers severe drawbacks, such as poor reproducibility and homogeneity of transistor char- acteristics, due to the peculiar laser process used forcrystallization [4]. Moreover, low-temperature polysilicon technology (LTPS) based on laser crystallization is far from being as mature as its amorphous silicon counterpart, and its acceptation by large display manufacturers is still poor.

In this paper, we present an alternative technology based on the use of silicon nanowires (NWs) that could bring the best of two worlds: low temperature and simple processing conditions, together with very good and stable transistor characteristics as can be expected from a monocrystalline semiconductor material.

Semiconductor NWs are a new class of materials currently studied within the context of molecular electronics. Typically, the diameter of such NWs ranges between a few nm and, say, 50 nm. Because of their excellent electrical characteristics, NW-based transistors could replace classical CMOS devices in the near future. For instance, mobility values as high as 1300 cm^2/Vs have been measured in p-type transistors fabricated from individual Si NWs [5]. Residual strain in the NW (leading to a reduction of the effective mass) probably accounts for this spectacular mobility increase compared to bulk Si [6] although more studies are needed to completely clarify this effect.

Since Si NWs can be grown and doped at low temperature ("'-4501C and below depending on the metal catalyst) using the vapour–liquid–solid (VLS) process [7], there is no need for refractory substrates. Moreover, some kind of crystallographic orientation control can be reached as a function of the Si NW diameter. According to a recent study, NWs with small diameters tend to grow along the /110S direction, whereas larger NWs tend to align along the /111S direction [8]. Hence there is no need for monocrystalline substrates either. For the above reasons, NW processing is totally compatible with glass-type substrates and NW-based devices will certainly soon be used as TFTs for active matrix backplanes in flat panel displays (LCDs and OLEDs) as well as in large-area X-ray imagers.

However, some of the major problems encountered so far with NWs are their manipulation, placement, and in-plane organization. Assembly by fluidic means [9] provides some kind of alignment, but no end-to-end registration. It is therefore difficult to precisely define and selectively dope the contact regions. This is the reason why transistors demonstrated so far have been using uniformly doped semiconductor NWs, resulting in high reverse leakage currents.

In this paper, we present a novel template growth method that we use to synthesize arrays of NWs in a reproducible way and with end-to-end registration. We use porous alumina membranes as a template material. In order to feed VLS growth, gold catalyst particles are first deposited at the bottom of the pores by an electrochemical process. However, the originality of the process we develop is that the pores of the membrane are forced to orient parallel to the substrate instead of perpendicular [10], a ''planar'' situation which is very convenient for device fabrication. Moreover, once grown in the pores of the array, the NWs can be collectively manipulated and organized by classical lithographic means.

The application of the method to active matrix back-plane fabrication for large-area imagers is presented and discussed below.

2. The VLS growth process

The VLS growth process has been extensively studied "'-40 years ago by Wagner [7] for the growth of whiskers. Concerning silicon, the growth mechanism can be explained with the help of Fig. 1. A gold dot (or gold cluster) is deposited on top of a chemically inert substrate and heated in a reactor at about 4001C, i.e., above the Au–Si eutectic melting temperature (see phase diagram in Fig. 1a). As silane (SiH_4) gas is allowed to flow over Au dot in the heated reactor, some SiH_4 molecules decompose by pyrolysis and some of the released Si atoms adsorb on the Au dot and form an alloy with the surface Au atoms. As more Si is brought to the Au surface, the alloy composition evolves towards the eutectic composition ("'-19 Si atoms%, see Fig. 1a). Melting starts to occur when the

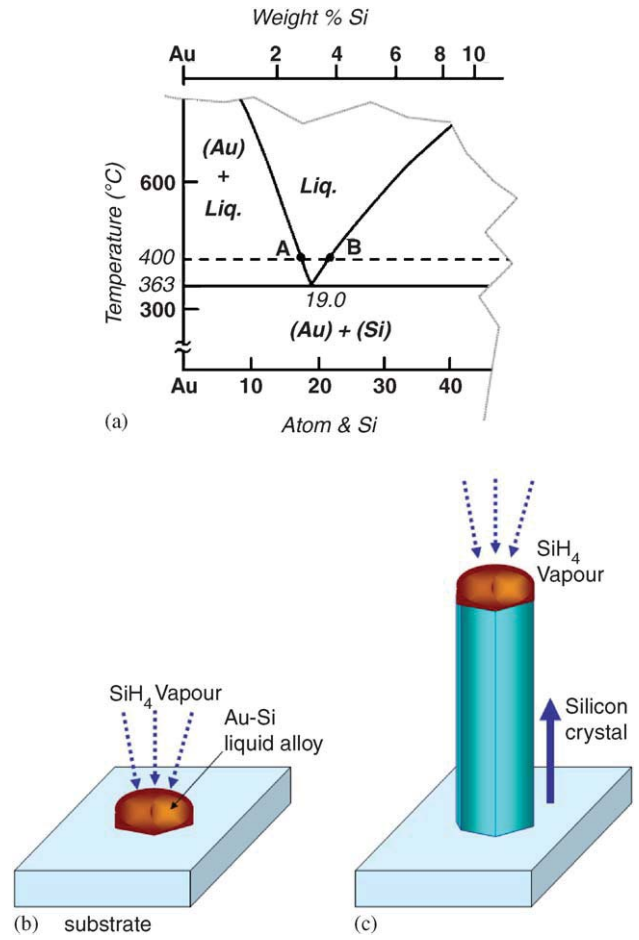

Fig. 1. Schematic mechanism of the VLS growth process: (a) Au–Si phase diagram; (b) and (c) formation of the liquid drop and growth of the Si whisker (see text for details).

vertical line corresponding to the actual composition reaches the point where the horizontal temperature line (say 4001C) intersects the liquidus curve of the phase diagram (point A), rapidly consuming the whole Au dot (Fig. 1b). Continued feed of Si makes the alloy composition evolve on the right-hand side of the eutectic point. Therefore, Si precipitation occurs when the alloy composition reaches a point where the liquidus line crosses again the horizontal temperature line (point B). An equilibrium is rapidly reached, where the flux of Si atoms incorporated at the surface of the liquid is balanced by the flux of Si atoms crossing the liquid–solid interface and precipitating. As the liquid surface behaves as an ideally rough surface, the sticking coefficient of the gaseous SiH_4 molecules is close to 1, resulting in a highly anisotropic growth that explains the whisker shape obtained (Fig. 1c). The Au–Si liquid drop rises on top of the crystal and appears spherical in shape due to surface tension effects.

The feasibility of Si NW growth by the VLS mechanism has been demonstrated recently using gold clusters [11]. Also, template growth in porous anodic alumina (PAA) has been used, in order to better control Si NW diameter [12,13].

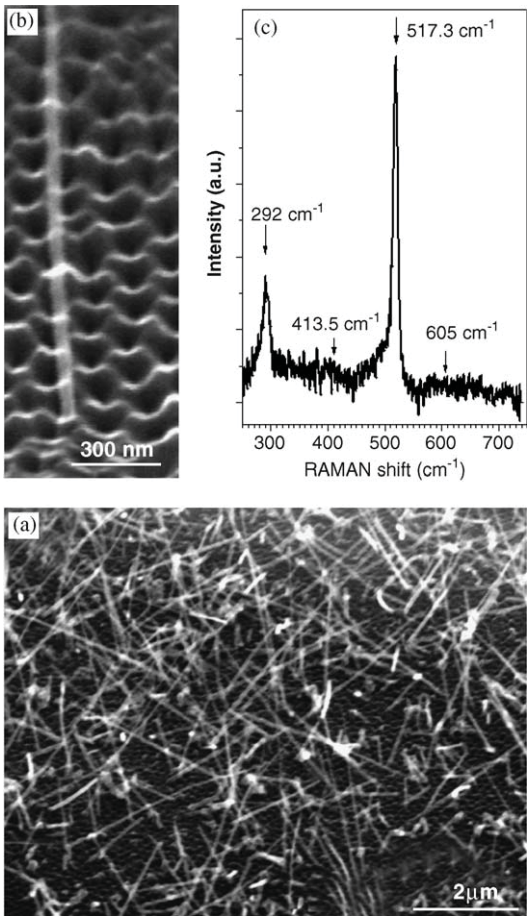

Fig. 2. (a) and (b) SEM characterizations of Si NWs grown in anodic alumina templates. The pore diameter was "-30 nm, and (c) Raman characterizations of Si NWs.

In Fig. 2, we present Si NWs grown in such templates. First of all, some kind of catalyst has to be deposited inside the pores. We have chosen gold as a catalyst and used the gold-mediated VLS method for the growth of Si NWs (see Fig. 1). In order to calibrate and optimize the Chemical Vapour Deposition (CVD) growth process, we have first used vertical porous anodic alumina templates easier to fabricate than the lateral ones.

Figs. 2a and b show some SEM observations of such Si NWs after growth. For these particular experiments, we have used porous alumina membranes synthesized with a pore diameter of "-30 nm, that can be easily observed with the SEM. We first note that the deposition of the gold catalyst inside the alumina pores is not uniform. In other words, there are less NWs on the membrane than emerging pores, which we believe is due to non-uniform deposition of gold inside the pores during the electrodeposition step. On the other hand, we observe that the diameter of the NWs is very uniform and regular over the sample (photographs taken over different parts of the sample are not shown here). Depending on the growth temperature, some parasitic amorphous silicon deposition can occur on the surface of the membrane, thus leading to a partial clogging of the pore aperture and inhibiting further NW growth. This can also be the reason why NWs do not grow in every pore.

Fig. 2b shows that the NW emerges from a pore, which strongly suggests that NW nucleation starts at the bottom of the pores, where the gold deposit is expected to lie.

The crystalline nature of the Si NWs is evidenced by Raman analysis using He–Ne laser excitation at $\mathbf{l}$ ¼ 632:8 nm, as presented in Fig. 2c. Typical Raman spectra of crystalline silicon (c-Si) exhibit a peak at 519.4 cm^{-1} which is the first-order optical phonon mode with the full-width at half-maximum (FWHM) at 4.5 cm^{-1}, whilst the second transverse optical phonon mode (2TO) peaks at 301.2 cm^{-1}. In the Raman spectra of Si NWs we present in Fig. 2c, there are four peaks at respectively 292, 413.5, 517.3, and 605 cm^{-1}. The most intense peak in the Si NWs is found to shift to a slightly lower frequency and to be asymmetric with a FWHM of 13.5 cm^{-1} notably larger than that of c-Si but in good agreement with previous reports on Si NWs [14]. The explanation is that the FWHM increase is associated with the disorder at boundaries (probably the periphery of the NWs) which leads to a decrease of the phonon life time. The two weak peaks at 604 and 423 cm^{-1} were found previously in Si nanoparticles [15] and porous Si [16], and they can be related to quantum confinement effects.

In summary, we believe that the Si NWs are monocrystalline as reported by others [5,11].

3. Transistor fabrication in lateral porous alumina templates

As quoted in the Introduction, we have recently developed a novel template structure based on PAA, where the pores grow parallel to the surface of the substrate instead of perpendicular, which greatly eases the contacting operations, as far as the fabrication of electronic devices is concerned [10,13]. Here, we would like to point out that depending on the anodic oxidation conditions (bath temperature, type and dilution of electrolyte, anodic voltage), the pore diameter of PAA templates can be controlled between "-5 nm and several 100 nm [17].

We propose to use our lateral anodic alumina templates to synthesize in a single CVD operation the basic structure of a TFT. This is explained in Fig. 3.

The pores of the lateral PAA are first filled with gold catalysts by electrochemical deposition (Fig. 3a). The samples are then loaded in a CVD reactor and NW growth is allowed to proceed, first with a mixture of SiH_4 and PH_3 or B_2H_6, resulting in the synthesis of n- or p-type doped NWs (Fig. 3b). The dopant gas is then suppressed, resulting in the growth of an intrinsic section of NW (Fig. 3c). Finally, the dopant gas is admitted again in the reactor and again mixed with SiH_4, resulting in a second doped section at the end of NW (Fig. 3d).

Note that the suppression and admission of the dopant gas (PH_3 or B_2H_6) can be gradual, thus resulting in

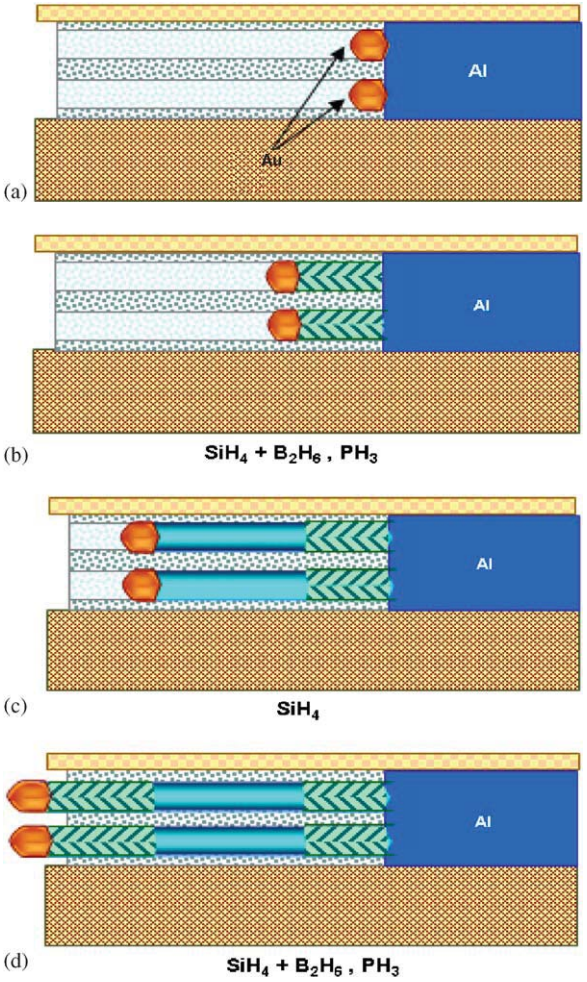

Fig. 3. The realization of a ''template'' TFT structure by CVD in only one ''pump-down'' operation: (a) lateral template with gold catalysts obtained by electrochemical deposition; (b) growth of the first contact region (mixture of SiH4 + dopant gas); (c) growth of the intrinsic channel region (pure SiH4); and (d) growth of the second contact (again mixture of SiH4 + dopant gas).

low-doped-drain (LDD) regions on each side of the transistor channel. Such structures are used to reduce hot carrier effects (when the transistor is in the on-state) and/or decrease the leakage current (transistor in the off-state).

The channel structure of the TFT, including the doped contact regions, is thus realised in only one pump-down, similarly to amorphous silicon technology [18]. However, in the present situation, the electrical characteristics of the TFTs (mobility in particular) are expected to be much better.

One advantage of the template growth method (horizontal or vertical) is that during deposition, only the tip of NW (where the Au–Si drop stands) is exposed to growth nutrients. Hence there is no possible contamination on the side walls of the intrinsic region of NW by unwanted PH_3 or B_2H_6 deposition when the second doped section is synthesized. Such unwanted deposition would lead to a short circuit between the source and drain regions of the TFT.

4. TFT incorporation in an active matrix and fabrication of an X-ray imager backplane

One of the challenges faced by display and X-ray sensor manufacturers is the reduction of the number of masks used for the fabrication of TFT plates. For instance, 5 masks are typically needed to manufacture the backplane of an active matrix liquid crystal display (AMLCD), a number that can be brought down to 4 if a diffractive mask is used for the fabrication of the TFT stack [18]. Concerning X-ray sensors, more masks are usually necessary because of sensor fabrication on the active matrix plane.

Figs. 4 and 5 show the main steps that we propose for the fabrication of an X-ray sensor panel with 3 TFTs per pixel,

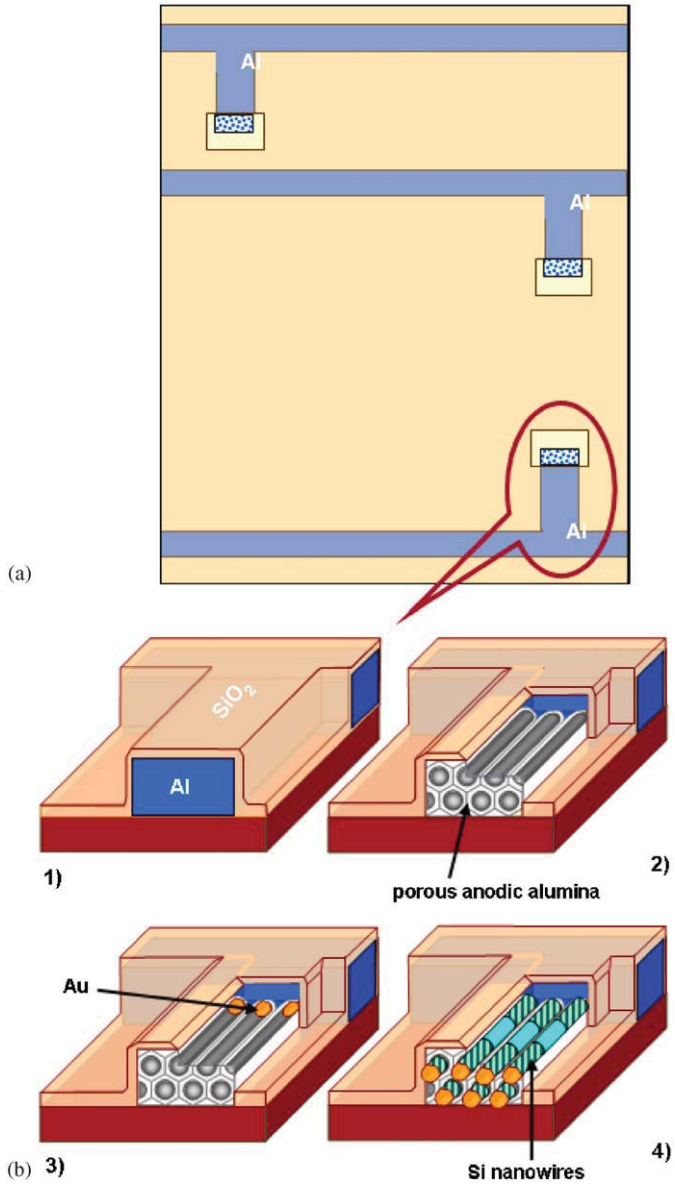

Fig. 4. TFT fabrication in an active matrix: (a) top view of the aluminum lines after deposition and etching followed by SiO_2 encapsulation and window opening; and (b) the fabrication sequence depicted in Fig. 2 performed in the Al fingers of Fig. 3a.

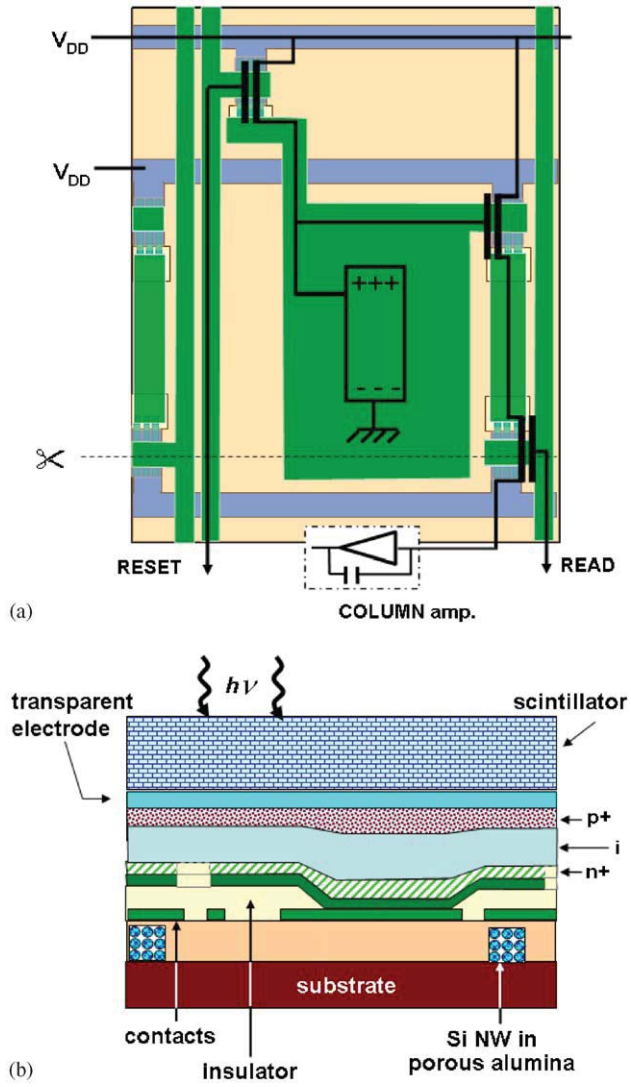

Fig. 5. (a) Pixel aspect after the first three mask levels and NW growth; and (b) cross section of the final structure.

namely an amplifier, a reset and a switch transistor. Aluminium lines are first deposited and etched (mask # 1), which exhibit 3 fingers in every pixel (see Fig. 4a). These lines are encapsulated with an insulator, e.g., SiO_2. The insulator is removed only at the tip of the Al fingers (mask # 2), thus exposing the end wall of the Al fingers (see Fig 4b, step 1).

All the Al lines are connected in parallel to a voltage source and the substrate is immersed in an electrochemical bath where anodic oxidation of the tip of the Al fingers is performed (Fig. 4b, step 2). Details of the anodic oxidation process can be found in Ref. [10]. Once the structure with the lateral pores obtained, gold catalysts are electrodeposited at the bottom of the pores and CVD growth of the transistor contacts and channel regions is performed (in one pump-down), as depicted in Fig. 3.

Fig. 5a shows the pixel structure after deposition and etching (mask # 3) of a second metal film. This metal provides gate contacts for the TFTs as well as drain contacts (the source contacts are the Al fingers) and some interconnections. The large pad at the pixel centre will serve to contact the bottom electrode of p–i–n capacitance. A second SiO_2 insulator is deposited and etched (mask # 4) over the central metal pad (see the cross section of Fig. 5b). Then the bottom electrode of p–i–n capacitance is deposited (metal # 3) and etched (mask # 5). The next step is the deposition of p–i–n stack, followed by a transparent electrode (Fig. 5b). Finally, the scintillator material is evaporated on top of the structure. Alternatively and in order to minimize the risk of lateral leakage, the bottom p–i–n electrode and the n+ layer are first deposited and then etched with mask #5. The intrinsic material, p+ contact and transparent layer are subsequently deposited.

Although the above description is probably over simplified, it shows that the mask count for an active matrix fabrication can be kept low, thanks to the TFT fabrication procedure in the lateral porous templates. In particular, only 5 masks are needed for the backplane fabrication of an X-ray sensor.

5. Conclusions

We have presented a novel TFT technology based on the use of semiconductor NWs grown at moderate temperature (around 400–4501C). Literature results show that transistors based on silicon NWs exhibit excellent transport and switching characteristics. Here, we grow the NWs in lateral alumina templates which makes them easy to handle and manipulate. The template structure provides a planar TFT arrangement, as well as end-to-end registration, which is very convenient for precisely locating the metal contact electrodes of the TFT. Modulation doping is also possible without artefacts, such as side wall doping of the NWs, and the basic TFT structure can be fabricated in only one CVD pump-down operation.

Finally, as far as the mask count for active matrix fabrication is concerned, our overall process is on the par with the most advanced amorphous silicon processes (which use a diffractive mask), and requires a reduced number of masking levels compared to LTPS technology.

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